What is Claimed is:

1. A method of detecting a long code composed from two shorter codes, the method comprising:

a)detecting the two shorter codes; and

b)based on the two detected shorter codes determining a phase of the long code.

2. The method of claim 1, wherein the long code is composed of symbols of the two shorter codes interleaved with one another.

3. The method of claim 2, wherein one of the shorter codes is n symbols long and the other one of the shorter codes is m symbols long, where m is greater than or equal to n and m and n are mutually prime.

4. The method of claim 2, wherein the two shorter codes are pseudonoise (PN) codes.

5. The method of claim 3, wherein $m=n+1$.

6. The method of claim 3, wherein a sequence of n symbols of the code m symbols long is identical to the sequence of the code n symbols long.

7. The method of claim 6, wherein the shorter codes repeat within a period of the long code.

8. A method of detecting from a received signal a long code composed from first and second codes interleaved with each other, wherein the first code has a length of n symbols and the second code has a length of m symbols, the method comprising:

a)demultiplexing the received signal into alternating symbol streams;

b)correlating the first symbol stream with a first reference code to produce a sequence of first correlation signals, and correlating the second symbol stream with a second reference code to produce a sequence of second correlation signals;

c)summing the sequence of first correlation signals over a first predetermined length to produce a first correlation sum, and summing the sequence of second correlation signals over a second predetermined length to produce a second correlation sum; and

d)processing the first and second correlation sums to produce a signal indicative of the phase of the long code.

9. The method of claim 8, wherein m and n are mutually prime.

10. The method of claim 9, wherein the first predetermined length is n symbols and the second predetermined length is m symbols.

11. The method of claim 10, wherein the first and second predetermined lengths are equal to n symbols.

12. The method of claim 10, wherein c) comprises:

c1) adding a current first correlation signal x1 of the sequence of first correlation signals with a rolling sum stored at a current address of a first rolling sum memory thereby generating a first sum, storing the first sum in the first rolling sum memory at the current address, and incrementing the first rolling sum memory's address modulo n;

c2) adding a current second correlation signal x2 of the sequence of second correlation signals with a rolling sum stored at a current address of a second rolling sum memory thereby generating a second sum, storing the second sum in the second rolling sum memory at the current address, and incrementing the second rolling sum memory's address modulo m;

c3) subtracting first and second sum delay values from the first and second sums, respectively, to generate first and second difference signals, wherein the first sum delay value corresponds to the (x1-n)th rolling sum and the second sum delay value corresponds to the (x2-m)th rolling sum;

c4) storing the first sum in a first sum delay memory at a current address of the first sum delay memory, and then incrementing the first sum delay memory's address modulo n•m; and

c5) storing the second sum in a second sum delay memory at a current address of the second sum delay memory, and then incrementing the second sum delay memory's address modulo n•m.

13. The method of claim 12, wherein d) comprises:

d1) delaying one of the first and second difference signals by a predetermined delay, and outputting first and second correlation sums;

d2) applying a merit function to the first and second correlation sums;

d3) determining the phases of the first and second short codes based on the merit function; and

d4) detecting the phase of the long code based on the phases of the first and second short codes.

14. The method of claim 12, wherein d) comprises:

d1) applying a merit function to the first and second correlation sums thereby generating first and second merit values;

d2) determining the phases of the first and second short codes based the first and second merit values; and

d3) detecting the phase of the long code based on the phases of the first and second short codes.

15. The method of claim 13, wherein the merit function comprises taking the product of the squares of the first and second correlation sums.

16. The method of claim 13, wherein the merit function comprises taking the minimum of the squares of the first and second correlation sums.

17. The method of claim 13, wherein the predetermined delay is one symbol.

18. The method of claim 13, wherein in b) the first and second symbol streams are correlated with at least n instances of the first and second reference codes,

respectively, each instance being delayed by a predetermined amount; and in d3) the phases of the first and second short codes are determined by identifying the amount of delay of the first and second reference codes that produces the sequence of correlation signals that results in first and second correlation sums that produce a merit function result in d2) that exceeds a threshold value.

19. The method of claim 13, further comprising determining a time of transmission of the received signal according to the detected phase of the long code.

20. The method of claim 13, comprising determining a range between a transmitter and a receiver that receives the received signal, according to the detected phase of the long code.

21. A computer-readable medium of instructions for detecting a long code composed from two shorter codes, comprising:

a) computer program instructions for detecting the two shorter codes; and

b) computer program instructions for determining a phase of the long code based on the two detected shorter codes.

22. The computer-readable medium of instructions of claim 21, wherein the long code is composed of symbols of the two shorter codes interleaved with one another.

23. The computer-readable medium of instructions of claim 22, wherein one of the shorter codes is n symbols long and the other one of the shorter codes is m symbols long, where m is greater than or equal to n and m and n are mutually prime.

24. The computer-readable medium of instructions of claim 22, wherein the two shorter codes are pseudonoise (PN) codes.

25. The computer-readable medium of instructions of claim 23, wherein m=n+1.

26. The computer-readable medium of instructions of claim 23, wherein a sequence of n symbols of the code m symbols long is identical to the sequence of the code n symbols long.

27. The computer-readable medium of instructions of claim 23, wherein the shorter codes repeat within a period of the long code.

28. An apparatus receiving a signal having first and second codes interleaved with each other, the apparatus comprising:

a correlator unit correlating the received signal with first and second reference codes corresponding to the first and second interleaved codes, respectively, and generating correlation signals;

an even code detector coupled to the correlator unit, for detecting from the correlation signals one of the first and second codes, and outputting an even code correlation signal;

an odd code detector coupled to the correlator unit, for detecting from the correlation signals one of the first and second codes not detected by the even detector and outputting an odd code correlation signal; and

a processing unit for processing the even and odd correlation signals to provide timing information.

29. The apparatus of claim 28, wherein the length of the first code is n symbols and the length of the second code is m symbols, where m and n are mutually prime.

30. The apparatus of claim 29, wherein the second reference code is the same as the first reference code.

31. The apparatus of claim 28, wherein the processing unit comprises:

a delay unit coupled to the even and odd code detectors, delaying at least one of the even and odd code correlation signals, and outputting a delayed correlation signal and an undelayed correlation signal; and

a merit function unit coupled to the delay unit combining the delayed and undelayed correlation signals according to a merit function; and

a timing unit coupled to the merit function unit for detecting a phase of the first code and a phase of a second code based on the combined correlation signals meeting a threshold value.

32. The apparatus of claim 28, wherein the processing unit comprises:

a merit function unit coupled to the even and odd code detectors and applying a merit function to the even and odd correlation signals thereby generating even and odd merit values; and

a timing unit coupled to the merit function unit for detecting a phase of the first code and a phase of a second code based on the even and odd merit values meeting a threshold value.

33. The apparatus of claim 32, wherein the timing unit determines, based on the detected phases of the even and odd codes, detects the phase of a long code formed from the interleaved first and second codes.

34. The apparatus of claim 31, wherein the merit function is the product of the squares of the delayed and undelayed correlation signals.

35. The apparatus of claim 31, wherein the merit function unit is the minimum of the squares of the delayed and undelayed correlation signals.

36. The apparatus of claim 31, wherein the timing unit determines, based on the combination of the delayed and undelayed correlation signals exceeding a threshold value, the phase of a long code formed from the interleaved first and second codes.

37. The apparatus of claim 36, further comprising a ranging unit for determining a range between the receiver and a transmitter of the first and second codes, based on the phase of the long code determined by the timing unit.

38. The apparatus of claim 36, wherein the correlator unit comprises at least two groups of correlators, the first group of correlators correlating symbols of the first code with a first reference code and the second group of correlators correlating symbols of the second code with a second reference code.

39. The apparatus of claim 31, wherein the even code detector comprises:

an even code rolling sum storage unit storing a plurality of rolling sums, and outputting one of the rolling sums;

an even code adder unit adding the rolling sum output from the even code rolling sum unit to a correlation signal generated by the correlation unit, and outputting a current even code rolling sum, wherein the even code rolling sum storage unit stores the current even code rolling sum;

an even code sum delay storage unit outputting a prior even code rolling sum, and storing the current even code rolling sum; and

an even code subtracting unit subtracting the prior even code rolling sum output from the even code sum delay storage unit from the current even code rolling sum, thereby producing an even code correlation sum signal.

40. The apparatus of claim 39, wherein the odd code detector comprises:

an odd code rolling sum storage unit storing a plurality of rolling sums, and outputting one of the rolling sums;

an odd code adder unit adding the rolling sum output from the odd code rolling sum unit to a correlation signal generated by the correlation unit, and outputting a current odd code rolling sum, wherein the odd code rolling sum storage unit stores the current odd code rolling sum;

an odd code sum delay storage unit outputting a prior odd code rolling sum, and storing the current odd code rolling sum; and

an odd code subtracting unit subtracting the prior odd code rolling sum output from the odd code sum delay storage unit from the current odd code rolling sum, and thereby producing an odd code correlation sum signal.

41. The apparatus of claim 40, wherein the odd and even rolling sum memories each store n and m rolling sums, respectively, and the odd and even delay memories store a multiple of n and m rolling sums, respectively.

42. The apparatus of claim 40, further comprising:

a first even counter outputting a first even count to the even rolling sum storage unit and the even sum delay storage unit;

a second even counter counting in response to an output of the first even counter and outputting a second even count to the even sum delay storage unit,

wherein the even rolling sum storage unit outputs the even rolling sum from a location addressed by the first even count and stores the current rolling sum in the location addressed by the first even count, and the even sum delay storage unit outputs the prior even code rolling sum from a location addressed by the first and second even counters, and stores the current even code rolling sum in a location addressed by the first and second even counters.

43. The apparatus of claim 42, further comprising:

a first odd counter outputting a first odd count to the odd rolling sum storage unit and the odd sum delay storage unit;

a second odd counter counting in response to an output of the odd counter and outputting a second odd count to the odd sum delay storage unit,

wherein the odd rolling sum storage unit outputs the odd rolling sum from a location addressed by the first odd count and stores the current rolling sum in the location addressed by the first odd count, and the odd sum delay storage unit outputs the prior odd code rolling sum from a location addressed by the first and second odd counters, and

stores the current odd code rolling sum in a location addressed by the first and second odd counters.

44. The apparatus of claim 43, wherein the first even and the second odd counters are modulo m counters, and the second even and the first odd counters are modulo n counters.

45. The apparatus of claim 44, wherein the first even counter is a modulo m counter the first odd counter is a modulo n counter, and the second even and second odd counters both together comprise a modulo p counter and a modulo q counter, where p•q is substantially equal to n and the modulo q counter counts in response to the modulo p counter, wherein the even sum delay memory is addressed based on the first even counter and the modulo q counter, and the odd sum delay memory is addressed based on the first odd counter and the modulo q counter.